Advanced Technology Information Processing Systems

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Fresh *THINKING*

ATIPS is an acronym for Advanced Technology Information Processing Systems. It's a name intended to convey the fact that our research spans a diverse field of interests, not limited only to analog or digital VLSI design. While the old VLSI group is now an integral part of the ATIPS group, our research continues to branch out in new directions – not the least of which are the pursuits of the Biomedical Microsystems Group (BMMG).

Photo courtesy "courtesy of Innovation Alberta with Cheryl Croucher

Our mission is to build a world-class research laboratory in the application of advanced fabrication technologies to problems in information processing systems. We provide the link between these emerging technologies and their various application areas, thus facilitating their rapid exploitation. More than simply building with what is available, we look for exciting new ways to integrate existing technology into cutting edge solutions.

Primary areas of concentration are VLSI technology, RF integrated circuits, MEMS and sensors, communication applications, signal processing applications, information security and computing systems. Within these areas, team members collaborate with industry innovators and leaders such as TRLabs, DALSA and Gennum.

The University of Calgary ATIPS Laboratory is supported by iCORE and is a member of the Canadian Microelectronics Corporation and Micronet.

DR GRAHAM A. JULLIEN

ADVANCED TECHNOLOGY INFORMATION PROCESSING SYSTEMS (ATIPS) LABORATORY

iCORE Chair
Electrical and Computer Engineering
University of Calgary

Dr Graham Jullien holds an iCORE Chair in Advanced Technology Information Processing Systems at the University of Calgary. iCORE has committed $800,000 per year for the first three years, then $600,000 per year for two years, for a total of $3.6 million dollars to establish this research team.

EXECUTIVE SUMMARY

The ATIPS Laboratory conducts research into the implementation of information processing systems using advanced and emerging technologies. The ATIPS laboratory provides a knowledge link between these technologies and the chosen application areas in order to both facilitate their rapid exploitation and to uncover new linkages. Our long-term goal is to apply advanced and emerging technologies to targeted applications by being knowledgeable and innovative at all steps in the process. To achieve this requires a group of multidisciplinary researchers who are prepared to interact at levels of knowledge beyond their own immediate expertise.

A major achievement this year has been to assemble such a group, the Centre for Innovative Wireless Integrated Microsystems (CIWIMS), and to define a CIWIMS Laboratory Cluster. The Cluster will provide a stimulating environment in which the researchers will interact to work on projects that require a much wider set of skills than are normally required for working in one specific research area. We currently have a group of 10 principal researchers from a wide range of areas including: wireless-RF; wireless-location finding; bio-sensors; System-on-Chip processors; thin-film and fabrication-integration; health sciences. The ATIPS Laboratory provides skill-sets in the general area of System-on-Chip processors, but our projects are collectively quite wide-ranging in scope, and oriented towards the targeted areas of wireless devices for the health sciences.

Our current projects include: wireless networks; embedded systems and fault tolerant systems; and the modeling and simulation of circuits and structures in advanced and emerging fabrication technologies. Highlights include: arithmetic techniques for applications as varied as low-power hearing instruments, 400M samples per second adaptive wireless base station filters, and extremely low noise digital processing circuits; machine vision techniques for analyzing defects directly within the camera in real-time; several novel video coding architectures for multi-media streaming.

Established research projects in the area of wireless networks include novel high signal rate filters for base stations and wireless "platforms" from which a variety of low-power mobile wireless devices may be quickly developed. We have also explored the areas of embedded and fault tolerant systems. This is a fruitful area for our group and we have conducted wide-ranging research into: machine vision; hearing instruments; arithmetic techniques; video processors and circuit techniques; along with novel methods that apply fault tolerance to computational systems with relatively low overhead. Finally we have linked this work with the advanced and emerging fabrication technologies with which we currently construct our microelectronic circuits.

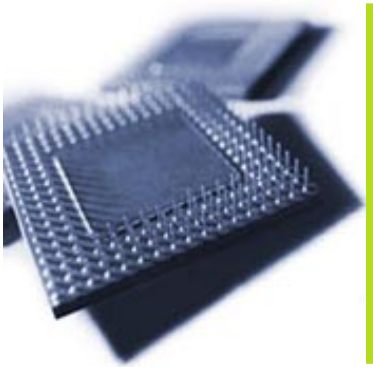
Our research is conducted with the support of major Canadian industries, and we are a member and lead client in the Canadian Microelectronics Corporation System-on-Chip Research Network, funded by a $40 million CFI grant, that is being used to bring the technology of System-on-Chip design to all interested Canadian universities.

The ATIPS Laboratory has a core personnel component of about 30 researchers and students. The laboratory workstations are host to approximately 100 graduate students and other users performing research on all aspects of microsystem design.

RESEARCH GOALS AND OBJECTIVES

The mission of the ATIPS laboratory is to investigate the use of advanced and emerging fabrication technologies to iCORE targeted applications in selected areas of information processing. The ATIPS laboratory provides a knowledge link between these technologies and the chosen application areas in order to both facilitate their rapid exploitation and to uncover new linkages.

The original targeted areas, based on the initial interests of iCORE, were: a) wireless networks; b) embedded systems including fault tolerant processors; c) computing with nanotechnology. We have contributed to each of these areas in a variety of ways, but have also targeted biotechnology and health sciences as major application areas. We formed a consortium, the BioMedical Microsystems Group (BMMG), at the University of Calgary, and this interaction has led to the establishment of the Centre for Innovative Wireless Integrated Microsystems (CIWIMS) and the assembly of the CIWIMS Laboratory Cluster in the new CCIT (Calgary Centre for Innovative Technology) building on campus. CIWIMS includes, among its principals, three iCORE Chairs (Dr Jullien, Dr Haslett, Dr Lachapelle), a Steacie Fellow (Dr Cannon), and a CRC Chair (Dr Okoniewski). In addition the group includes Dr Kaler, the Director of the Calgary Institute for Nanotechnology (CINT), with strong ties to the National Institute for Nanotechnology (NINT) at the University of Alberta, and two very promising young faculty members (Dr Badawy, an ATIPS Laboratory member, and Dr Budiman, a thin film specialist from the mechanical and manufacturing engineering department). The health sciences are represented by two outstanding scholars (Dr Sheldon and Dr Pilarski) from the Medical Faculties at, respectively, the University of Calgary and the University of Alberta. The ATIPS Laboratory also has close ties with the mathematics department at the University of Calgary; in particular the cryptography group led by iCORE Chair, Dr Hugh Williams. Dr V.S. Dimitrov (ATIPS iCORE Associate) and Dr G. Jullien are members of the Centre for Information Security and Cryptography (CISAC), founded by Dr Williams; Dr Dimitrov has been elected to the board of CISaC as the Faculty of Engineering board member.



OUR LONG-TERM GOAL IS TO APPLY ADVANCED AND EMERGING TECHNOLOGIES TO TARGETED APPLICATIONS BY BEING KNOWLEDGEABLE AND INNOVATIVE AT ALL STEPS IN THE PROCESS. TO ACHIEVE THIS REQUIRES A GROUP OF MULTIDISCIPLINARY RESEARCHERS WHO ARE PREPARED TO INTERACT AT LEVELS OF KNOWLEDGE BEYOND THEIR OWN IMMEDIATE EXPERTISE.

Wireless Networks

A research project on adaptive filters is being conducted in cooperation with TRLabs, Calgary. The application is an experimental 1.2Gbps wireless LAN (local area network) operating at a frequency of 17Ghz. The system is asymmetrical, which means that most of the processing power is contained in the fixed base-station with very little (mostly analog) circuitry contained in the mobile units. This project is involved with the application of special number theoretic techniques to the implementation of high-speed quadrature signal adaptive filters. A novel processor design has been been tested on a custom FPGA (field-programmable gate array) simulator, developed by TRLabs (Calgary), at somewhat lower speeds than required for the final design. An IP Core (proprietary processor block) in 0.18µ CMOS is being designed to operate at the planned throughput of 400M samples per second.

A new research project on System-on-Chip low-power wireless platforms was started in 2002. The work involves developing versatile wireless enabled integrated circuit design structures (platforms) to which custom functionality can be added. This research is being conducted as part of the University of Calgary lead-client status for the Bluetooth IP core and IP core authoring threads associated with the CMC SoC Research Network (SOCRN). This work also formed part of a tutorial presented at the 2003 International Symposium on Circuits and Systems by W. Badawy (Calgary), Y. Savaria (École Poly.) and G. Jullien (Calgary).

Machine Vision

We have conducted a long-term project on multiple camera defect detection on rolling conveyor processes. The systems use multiple synchronized cameras in order to cover large width conveyors with pixel sizes in the tens of microns. Our current work involves the use of line-scan TDI (time delay and integration) CCD (charge-coupled device) sensors, with video stream FPGAs, We have recently demonstrated the ability to self-synchronize the CCD sensors with the image velocity using only the output of the sensor (prior to this development it was necessary to use optical shaft encoders connected to the conveyor). The control of the synchronization has been coupled with defect detection algorithms implemented in the on-line FPGAs, to produce a very versatile set of techniques for defect detection in heavily textured backgrounds. This work involves close interaction with an industrial sponsor (DALSA Inc.).

As part of our work on machine vision we have recently investigated the use of plenoptic cameras for single camera depth recovery. A customizable plenoptic camera simulator, using backward ray tracing with stochastic sampling, was developed in 2002. This simulator will enable our research group to test any plenoptic camera configuration for depth recovery purposes. The simulator has been successfully tested against standard camera-lens configurations and we are now looking at potential plenoptic configurations for building a custom test camera system.

Hearing Instruments

This work is sponsored by our industrial partner, Gennum Corporation, and is related to the application of special architecture, arithmetic and circuit techniques to producing very low-power programmable digital implementations. Completely in the Canal (CIC) hearing instrument devices are particularly challenging to digitize because of the extremely small size and power dissipation required. Our goal is to continue and extend this work to embrace our wider interests in microconvergent systems.

In 2002 a hearing instrument filterbank processor was designed, fabricated in 0.18µ CMOS, and tested. The processor uses a 2-D 2-digit multi-dimensional logarithmic number system (MDLNS) to implement the filterbank. A binary to MDLNS converter, using a completely new conversion technique, was also implemented on the chip. The chip has been successfully tested and the technique is now being examined by our sponsor for potential commercialization.

We have also recently commenced a project on developing an asynchronous MDLNS processor architecture in order to further lower the power dissipation, and to reduce the effects of switching noise due to clocking. A complete asynchronous architecture for the MDLNS processor has been developed, including an asynchronous control system for realizing handshaking protocols. Full-custom integrated circuit cells have also been developed for future fabrication of a test chip.

Next-generation hearing

instruments will be based on the directivity obtainable with microphone arrays. In a joint project with the University of Windsor and Gennum Corp. we have developed designs for MEMS microphone arrays, special MEMS sockets for integrating the MEMS arrays with integrated circuit processors, and techniques for using them in acoustic beam steering. We are currently converting the original designs into process steps for implementing at the University of Alberta NanoFab. This work will be among the first of our microconvergent research projects.

Arithmetic techniques

One of our long-term strengths is the investigation of alternative techniques for number representation in order to reduce the complexity and improve the performance of real-time digital signal processing systems. We define performance in terms of cost functions containing: time delay; resource utilization (e.g., silicon area or FPGA logic blocks); power dissipation; system noise (particularly with mixed-signal designs that use noise sensitive analog circuitry); and design time (with particular emphasis on SoC design reuse using parameterizable processor blocks).

In a direct link between arithmetic architectures and deep-submicron (DSM) technologies, we have been working on a variety of multiplier structures in terms of the effect of interconnect wiring on their performance. We have recently established optimum multiplier architectures for a variety of DSM technologies.

We are currently investigating the application of a multi-dimensional logarithmic number system that has been in development by our group for the past three years. It is based on earlier work on a double-base representation, pioneered by iCORE Research Associate, Dr Vassil Dimitrov, and our research group at the University of Windsor. We have developed a complete theory for this new number representation and have applied it to several application areas.

Many digital signal-processing computations are based on coefficients that are irrational (particularly transforms such as DFT, DCT and also some wavelets). In implementing these computations, we invariably introduce errors because of the need to represent the coefficients with finite precision. Our group has recently investigated mapping techniques, based on the use of algebraic integers, which allow the manipulation of such coefficients without any error. So far, we have applied our technique to DCTs and wavelets, with applications to video compression.

An increasing concern in DSM technologies is the noise generated by the very short switching transients in digital circuitry. In systems that combine sensitive analog circuitry (for example circuitry associated with sensors), this switching noise can be a major problem. We have taken a completely different approach to this problem by defining arithmetic systems that compute with digital precision but only use standard analog circuits. We have recently developed two such systems; one is based on cellular neural networks (non-linear analog circuits in a 2-D array); the other, in collaboration with the RCIM research group at the University of Windsor, is based on a natural analog representation of multi-digit numbers – continuous valued digits. We are currently developing test circuitry to further evaluate these arithmetic systems.

Video Processors

Streaming video has become ubiquitous on the Internet. Given typical Internet bandwidths to the consumer, there is a need to greatly compress the video data in order to provide streaming capabilities without interruption (current techniques compress by about 2-orders of magnitude). Our interests are in the efficient implementation of current compression standards, including discrete cosine transforms (DCTs) and discrete wavelet transforms (DWTs), and the development of new standards. iCORE Research Associate, Dr W. Badawy, is a Canadian representative on the MPEG4 standards committee.

We have used the algebraic integer work from our arithmetic investigations to implement error-free DCTs and have extended this concept of multidimensional algebraic integers Daubechies DWTs. A DCT chip is currently undergoing testing in order to verify the simulated performance.

Dr W. Badawy, iCORE Research Associate, has also explored novel video and image coding architectures, for the MPEG4 and JPEG2000 standards, using more conventional arithmetic techniques. For these architectures we have implemented both DWTs and DCTs. One of the DWT designs was submitted to the MPEG4 (Part 9) Committee,

and another design, based on distributed arithmetic (DA), was proposed in which the performance improved on the best existing architectures by 40 percent. A new DCT time distributed architecture was proposed and successfully implemented using FPGAs. This design was also submitted to the MPEG (Part 9) committee and was accepted as a reference architecture and code for an MPEG4 hardware profile.

Circuit Techniques

Where necessary we look at designs at the transistor level. In the past this has included special dynamic logic circuitry and minimized transistor tree structures. Our current interests are in the use of non-linear analog circuits implementing cellular neural network (CNN) array architectures. CNN arrays allow digital computation with very low system and cross-talk noise (three orders of magnitude below CMOS) because of the continuous dynamics of the interconnected non-linear analog cells. We are exploring a variety of number representations including standard binary, signed digit (using bi-directional current circuits) and DBNS. Dr J. Haslett, TRLabs/iCORE/NSERC Industrial Research Chair in Wireless RF Integrated Circuit Design, is co-supervising a student in this work and our results are being prepared for publication.

Fault Tolerant Systems

Fault tolerance is important for systems that have to operate reliably over long periods of time. Fault tolerance may also become important as fabrication densities increase to the point where the potential of soft faults increases. We have recently developed low overhead (about 30 percent) fault tolerant computational arrays based on the MRRNS system; this representation is also used to implement the adaptive filter for the TRLabs experimental LAN, and we plan to add fault tolerance to the base station adaptive filter during the next year.

Advanced Technologies and Computing with Nanotechnology

Our interests in advanced CMOS technologies are in the development of novel designs, from system level to transistor level. With this vertical approach we encounter a variety of design challenges. As technologies advance, device densities increase and each level in the design hierarchy brings its own problems and requires different solutions. The amalgamation of these design solutions and advanced technology modeling constitute System-on-Chip design. In the past few months we have set up a design laboratory, with both physical and electronic security, to enable our team to explore and develop SoC designs with third party IP blocks and advanced tools from the Canadian Microelectronics Corporation. We have also started to look at design reuse as a powerful tool for our own novel and custom designs.

The technology that has brought us advanced integrated circuits is also responsible for other microstructure-based technologies, including MEMS, microfluidics, RF-wireless components, and photonic devices. These technologies are, in the main, disparate but very useful microsystems can be built using the microconvergence of these technologies. We have assembled a consortium of researchers to examine the application of wireless enabled microconvergent systems, with particular applications in biotechnology and the health sciences. We have already started to develop several bio-MEMS blocks, including starting work on a low-power bio-platform. The first application of this platform will be to implement a novel "lexel" array, in conjunction with the bio-electric laboratory, directed by Dr K.V.I.S. Kaler, that is to be used as a dielectrophoretic cell analysis technique.

Computing with Nanotechnology

Our interests in the use of nanotechnology for computing are somewhat different to the burgeoning research into quantum computing. We are interested in exploring nanotechnologies that will provide a fairly smooth design space transition from design techniques used for conventional FET-based circuitry. We have initially targeted quantum cellular automata (QCA) technology for our studies, since it has been rated by several research organizations in the top six of nanocomputing technologies that have the most promise for commercial fabrication. The arrays of quantum dots that make up each QCA cell can also operate in a 2-state mode, which provides a smooth design transition from the low/high impedance states of FET channels that are used to implement 2-state logic in conventional designs. We have had considerable initial success with a unique CAD tool (QCADesigner) for quantum

cellular automata (QCA) architectures. The tool is unusual in that, although the technology is rather speculative at the moment, we have sufficient modeling information with which we can develop and simulate architectural blocks that we typically find in processor architectures built with standard integrated circuit fabrication technology. We have built the tool using a simulator jointly developed with the research group at the University of Notre Dame in Indiana – the group that initially proposed QCA technology. QCADesigner received the Micralyne Microsystems Design Award at the 2002 CMC Workshop. The tool has been used, by our group and many other researchers, to design new structures for potential QCA architectures. Springer has invited our group to write a textbook on the technology, QCADesigner and our new structures.

RESEARCH TEAM

Part of the ATIPS research program is being conducted by students at Dr Jullien's previous institution, the University of Windsor. These students are funded from Micronet grants.

TEAM LEADER	AWARDS
Graham Jullien	Elected IEEE Fellow
TEAM MEMBERS	**TITLE**
Vassil Dimitrov	iCORE Research Associate; Number representations, Digital signal processing
Wael Badawy	iCORE Research Associate, VLSI Architectures, SoC, Image recognition, Low-power design
LABORATORY MANAGERS	**POSITION**
Jonathan Eskritt	ATIPS Lab Manager
Paul Hobal	ATIPS Webmaster and Publicity Manager

POSTDOCTORAL FELLOWS	TOPIC
Peiyu Zhang	Bio MEMS, Optical MEMS, MEMS Processes, Clean Room procedures
Wenjing Zhang	Data Stream SoC Architectures, VLSI Design, Integrated Circuit Test, Neural Networks

PHD CANDIDATES	TOPIC	AWARDS
Ibrahim Baykal	Defect Detection using in-Camera Video Stream Processing	
Jonathan Eskritt	Applications of programmable complex base MDLNS representations	
Minyi Fu	Applications of Algebraic Integers in New Architectures for Video Codecs	
Youssef Ibrahim	Analog Cellular Neural Networks for Redundant Arithmetic Ultra Low-Noise Processors	Ontario Graduate Scholarship
A. Makki	Beam-Steered Hearing Instruments	
Roberto Muscedere	Difficult Operations in Double-Base Number Systems	
Konrad Walus	Quantum Cellular Automata	NSERC PGS-A, iCORE Graduate Student Scholarship

MSC CANDIDATES	TOPIC	AWARDS
Mehboob Alam	SoC Implementation of Video Codecs	
Mohamed Amtoun	Depth Recovery in Plenoptic Cameras	
James Doherty	Transcutaneous Powering of an Implantable Stimulator	Alberta Ingenuity
Ryan Glabb	Low-power System-on-Chip Platforms	
Paul Horbal	Adiabatic logic for ROM-Based Architectures	

Jeffrey Keilman	Lexel Arrays for Cell Manipulation using Dielectrophoresis	NSERC PGS-A, iCORE Graduate Student Scholarship
Jennifer Li	An MDLNS Filter-bank for a Low-power Digital Hearing Instrument	
Pedram Mokrian	Multiplier Design in Deep Sub-micron Technologies	
Arash Razavi	Plenoptic Camera Optical Path Simulation using Stochastic Sampling Techniques	
Mohammed Sayed	Embedded Memory Architectures for MPEG4 Motion Estimation	
Gabriel Schulhoff	Modeling Quantum Dots on a Computer Cluster	
Jeff Tracey	Optimized Arithmetic Cells for SoC IP Blocks	
Jiansong Wu	Asynchronous Hearing Instrument MDLNS Processors	
Jonathan Yeboah	CNN Analog Circuits for Ultra Low-Noise Digital Adder Design	

UNDERGRADUATES	TOPIC
Ian Steiner	MRRNS Complex Arithmetic Adaptive Filter: Quantized Polynomial Number Representation
Adesh Garg	MRRNS Complex Arithmetic Adaptive Filter: Simulation and Evaluation

COLLABORATIONS

RESEARCH COLLABORATION

University of Windsor, Ontario. G.A. Jullien has a formal association with the Research Centre for Integrated Microsystems. Research colleagues are M. Ahmadi and W.C. Miller and we are co-applicants on a $53,000 Micronet grant (principal applicant M. Ahmadi - S.1.WI). M. Ahmadi is also a co-applicant on a $213,000 Micronet Grant (S.2.CAL - G.A. Jullien principal applicant). G. Jullien currently supervises or co-supervises six graduate students (three other graduate students supervised or co-supervised in 2002 have since graduated). Our area of research is in hearing instruments, MEMS, and signal processors.

Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, France. G.A. Jullien and V.S. Dimitrov, have a strong research association with Dr L. Imbert (CNRS Researcher) and Dr J-C. Bajard (Director of the Dept. Fundamental and Applied Informatics). Dr Imbert was employed as a postdoctoral fellow in both Windsor and Calgary, and G. Jullien has visited Dr Bajard at Montpellier and also his previous laboratory in Marseilles. We currently have a joint French-Canadian research grant application under review (applicant V.S. Dimitrov). Our areas of research are computer arithmetic, cryptography, and fault tolerance. A joint paper has been accepted for publication this year.

Helsinki University of Technology. Dr V.S. Dimitrov has strong ties with GETA (Graduate School in Electronics, Telecommunication and Automation). He was a consultant there from 1997-2000 and has taught short courses at GETA from 1998 to the present. G. Jullien has also taken part in one of the earlier short courses. (http://wooster.hut.fi/geta/courses/graham/index.html). The areas of research are DSP, number theoretic techniques and cryptography.

The Queen's University, Belfast. G. Jullien has had ties with two colleagues in the Department of Electrical and Electronics Engineering at Queen's for several years. Dr J. McCanny CBE, FRS, FIEEE, interacts with Dr Jullien in the area of systolic arrays and IP cores for signal processing. Recent discussions have taken place regarding the acquisition of IP cores from Amphion Inc, where Dr McCanny is CTO. These discussions have involved CMC and the SOC Research Network. Dr McCanny was one of the plenary speakers at the IWSOC workshop at Banff, where G. Jullien was the general chair. He also acted as a consultant to the ATIPS Lab. in 2002. The other colleague is Dr J. Woods in the area of rapid prototyping and FPGAs. Dr Jullien was invited to Queen's as a distinguished scholar in 1999, and Dr Woods is being invited as a consultant to the ATIPS Laboratory in October, 2003.

The University of Lousiana at Lafayette. Dr Jullien has had ties with the Centre for Advanced Computer Studies (CACS) since the late 1980s. The chair of both the departments of electrical and computer engineering and computer science, Dr M. Bayoumi, is a former student of Dr Jullien, and Dr Badawy received his PhD under Dr Bayoumi's supervision. Dr Jullien has acted as both consultant and distinguished lecturer at CACS and Dr Bayoumi will be visiting the ATIPS Lab this year as a consultant. The research area of interest is in digital video processing and integrated circuit design.

The University of Texas at Austin. Dr Earl Swartzlander, of the department of electrical and computer engineering, has had strong ties with DrJullien's research group over the past 17 years. Dr Swartzlander and Dr Jullien have been involved in the organization of several conferences in the area of array processing and computer arithmetic, and Dr Swartzlander was a plenary speaker at the IWSOC in 2002. They have had previous joint papers together in the area of transistor level circuits for computer arithmetic.

The University of Grenoble, Spain. Dr Antonio Garcia, ECE. Dr Garcia was a research associate in G. Jullien's laboratory in the late 1990s, and they have continued to work together on parallel processors using modular arithmetic. A joint paper was presented this year.

The University of Wisconsin, Madison. Dr Jullien has collaborated on conference organization and a special journal issue with Dr M. Schulte, in the department of electrical and computer engineering. The special issue was based on the 2001 ASAP conference, and Dr Schulte is the technical chair for the 2003 Asilomar Conference on Signals,

Systems and Computers, for which Dr Jullien is the general chair.

Other collaborations. For brevity we list other university collaborations together in this section with contacts and research areas. All collaborations have either resulted in visits to discuss research projects, or the organization of special sessions at conferences.

- University of Newcastle, UK - Dr N. Coleman (logarithmic processors).
- University of Cardiff, Wales - Prof. N. Burgess (residue number systems).
- Penn State, US - Prof. W.K. Jenkins, Chair ECE (computer arithmetic).
- UCLA, Dept. Computer Science - Prof. M. Ercogovac, Chair (computer arithmetic).
- University of Florida, Gainesville - Dr F. Taylor, ECE (real-time architectures).
- Edith Cowan University, Perth, Australia - Dr K. Eshraghian, Head of School and Foundation Professor of Computer, Communication and Electronic Engineering (VLSI design, processor architectures).
- Universita' degli Studi di Trento - Dr Andreas Caranti, Dept. Math. (number representations, cryptography).
- Notre Dame University, Indiana - Dr Craig Lent, Microsystem Group (Quantum Cellular Automata).

COLLABORATION WITH INDUSTRY

DALSA Inc.

Dr Jullien and his research team have had a long-term research interaction with DALSA Inc. Dr Jullien helped pioneer the concept of in-camera defect detection with DALSA engineers, and this work has led to significant sales in the area of defect detection in web manufacturing processes. The concept was transferred to a university project supported by Micronet with industrial funding from DALSA (approximately $500,000 over the past decade including matching funds).

Gennum Corp.

Dr Jullien's laboratory at the University of Windsor, and now extended to the University of Calgary, has been working with Gennum Corp. since 1994. The initial work, which is still on-going, was in the area of video signal processing (for broadcast quality TV signal processing). Since 1998 our group has worked with Gennum Corp. on hearing instrument processors. Since 1994, Gennum has contributed over $700,000 (including matching funds) to our research.

TRLabs

We have included TRLabs in this section since part of its funding comes from industry. TRLabs has sponsored the ATIPS Laboratory since its inception. Currently, an intern student is partially supported from TRLabs funding (see the Research Projects section).

City of Calgary

Dr Badawy has been applying his novel work on vision systems to the development of an Active Camera Tracking System for Traffic Analysis. The City of Calgary is contributing $120,000/year and also allowing special access to traffic lights and infrastructure.

IPROS

This start-up company in Toronto invited Dr Dimitrov to be on its advisory board. The company is working on building SoC cores for the efficient implementation of complex arithmetic processors, for applications in smart antennas for the communications market.

We have several other industrial contacts as follows: Qinetiq, UK, this used to be a UK Government institution (the Royal Signals and Radar Establishment), but has now been privatized. We have connections with Dr J. McWhirter, FRS, Dr I. Proudler and Dr R. Walke in the area of array processors for DSP. Dr McWhirter will be the plenary speaker at the 2003 Asilomar Conference, and has also been invited to visit the ATIPS Laboratory, as a consultant, in October 2003. We have recently made contacts with the following local industries: Smart Technologies Inc., SiWorks, and Non-Elephant Encryption Systems. We are also interacting with the Innocentre and organize an annual Lunch'n Learn meeting to introduce local industry to the projects and capabilities of the ATIPS Laboratory.

MULTIDISCIPLINE OR MULTI-INSTITUTIONAL PARTNERSHIPS

Micronet R&D (NCE)

Dr Jullien was one of the founding members of Micronet, one of the first 14 Networks of Centres of Excellence, and one of only five to be funded through the full 14 year life-span of networks in the NCE program. Dr Jullien

sits on the Board of Directors, the Steering Committee, and the Coordinating Committee of Micronet. Micronet R&D is comprised of 17 universities, 44 companies and two federal organizations, all in Canada. The research personnel contributed by the universities includes 71 faculty members and 363 graduate students and other research personnel. For 2001-2002, the total income of the network was $4,306,000 with approximately 32 percent being contributed by industry. Dr Jullien leads a project which was funded at $213,000 in 2002 (made up from Micronet base funding, industrial contributions and funding from the NSERC eMPOWR Innovation platform). This is one of the largest of the more than 50 projects funded by Micronet. In addition, Dr Jullien is a co-applicant in a second project from the University of Windsor, funded last year at $53,000. Until 1998, Dr Jullien was also the principal investigator in this second project.

Canadian Microelectronics Corp. (CMC)

CMC provides microsystem design tools, and fabrication and information services to 44 Canadian universities, and colleges. It has 25 Canadian companies as members and is strongly linked to industry organizations and has a senior government official on the Board. Dr Jullien has been a member of CMC since 1985 (less than a year after it was founded). He served as Member Representative for the University of Windsor until 2000. He was on the Board of Directors from 1989-93 (vice-chairman of the Board in 1993) and rejoined the Board in 2001. He is one of 10 principal researchers in the System-on-Chip Research network, funded by a $40M CFI grant. Drs Badawy and Jullien are lead clients for the IP blocks that were purchased from the CFI funds, and the IP block authoring suite being developed by a sub-committee of the Technical Advisory Committee. A secure laboratory has been set up in the CCIT building to handle commercial IP blocks in the development of SoC platforms.

The Centre for Information Security and Cryptography (CiSAC)

Prof. Hugh Williams, iCORE Chair in Cryptography, Department of Mathematics at the University of Calgary has established CiSAC to bring together a multidisciplinary interest group in the area of cryptography and quantum computing. Drs. Dimitrov and Jullien are members of this centre and Dr Dimitrov also sits on the board of CiSAC as the Engineering Representative.

FUNDING

Our work is supported, in addition to iCORE, by NSERC, the Canadian Microelectronics Corporation, Micronet R&D (NCE), and several prominent microelectronic industries.

In addition to the iCORE funding of $800,000, the budget includes grants at $149,000 NSERC and $213,000 from the Micronet NCE project (includes Micronet base funding, industrial contributions and NSERC eMPOWR funding).

New funds acquired as co-investigator include $53,000 from Micronet NCE, with M. Ahmadi as principal investigator Canadian Microelectronics Centre for the SoC Research Network.. Dr Jullien is one of 10 principle researchers in the $40 million four-year System-on-Chip Research Network.

INTELLECTUAL PROPERTY

Since the ATIPS Laboratory became operational in mid-2001, we have been in close contact with University Technologies International, wholly owned by the University of Calgary, and have been encouraged to protect any substantial IP that is developed as part of research projects undertaken in the ATIPS laboratory. ATIPS accepts this encouragement in the case of substantive intellectual property opportunities.

Activity this year, including revenue

There has been no revenue from intellectual property this year since we have only just started IP protection procedures. ATIPS is recording the following activities connected with IP protection and development:

i) Optimal base 2-D logarithms for very efficient FIR filter implementations – submitted to UTI for patent consideration. (Dimitrov-Jullien)

ii) Double-base sparse representations for applications in Cryptography – submitted to UTI for patent consideration (Dimitrov-Jullien)

iii) Self-synchronization algorithms for time-delay and integration (TDI) line-scan cameras for machine vision applications – submitted to UTI for patent consideration (Jullien)

iv) Lexel arrays for arbitrary electric field generation with applications to cell motion and identification using dielectrophoresis – submitted to UTI for patent consideration (Jullien-Kaler)

v) Trade Names LEXEL and PLEXEL submitted to UTI for registration (Jullien-Kaler)

vi) Two other trade names have been registered with UTI; GrApp and WebConcorde. These are associated with a software package developed for hosting technical conferences and paper/review submissions on the web (Badawy)

vii) A potential startup company on Vision Systems has been registered with InnoCentre for the purpose of attracting venture funding (Badawy)

PUBLICATIONS

Refereed Journal Publications

1. V.S Dimitrov and G.A. Jullien, "Multidimensional Algebraic-Integer Encoding for High Performance Implementation of the DCT and IDCT," *Electronics Lett.*, vol.39, no. 7, 2003, pp. 602-603.
2. W. Badawy, M. Talley, G. Zhang, M. Weeks, and M. A. Bayoumi, "Low power very large scale integration prototype for three-dimensional discrete wavelet transform processor with medical applications," *The SPIE Journal on Electronic Imaging*, Vol. 12, No. 2, April 2003, pp. 270-277.
3. K. Wahid, V.S. Dimitrov, G.A. Jullien, and W. Badawy, "Error-free computation of Daubechies Wavelets for Image Compression Applications," *Electronics Lett.*, vol.39, no. 5, 2003, pp. 428-429
4. Arash Shoarinejad, Sue Ann Ung, and W. Badawy, "Low power single-bit full adder cells," The *Canadian Journal on Electrical and Computer Engineering*, Vol. 28, No. 1, January 2003 pp. 3 - 9.
5. Wael Badawy and Magdy Bayoumi, "A Parallel Multiplication-Free Algorithm and Architecture for Affine-based Motion Compensation," *The SPIE Journal on Optical Engineering*, Vol. 42 No. 1, January 2003 pp. 255 - 264.
6. A. Saed, M. Ahmadi, and G.A. Jullien, "A Number System with Continuous Value Digits and Modular Arithmetic," IEEE *Trans. on Computers*, vol. 51, no. 11, 2002, pp. 1294-1305.
7. J.M.A.Tanskanen, and V.S. Dimitrov, "Round-off Error-Free Fixed-Point Design of Polynomial FIR Predictors and Predictive FIR Differentiators," *Digital Signal Processing*, vol. 13, 2002, pp. 42-57.

8. Hesham Ahmed, Walied Moussa, Wael Badawy, Medhat Moussa, "Applying FEA to Investigate the performance of Electrostatic Comb-Drive Actuators Utilized by on-a-chip systems", *The Canadian Journal on Electrical and Computer Engineering*, Vol. 27, No. 4, October 2002, pp. 195 - 200.
9. A. Garg, G.A. Jullien, G.H. McGibney, and J.W. Haslett, "A Modulus Replication Complex Adaptive Filter IP Core," *Canadian Journal of Electrical and Computer Engineering*, vol. 27, no. 4, 2002, pp. 177-181.
10. M. Sayed and W. Badawy, "A Novel Low Power Embedded Memory Architecture for MPEG-4 Applications with Mobile Devices," *Canadian Journal on Electrical and Computer Engineering*, vol. 27, no. 4, 2002, pp. 171-175.
11. W. Badawy, "System on Chip: the future of System Integration," *Canadian Journal on Electrical and Computer Engineering*, vol. 27, no. 4, 2002, pp. 149-154.
12. H. Safiri, M. Ahmadi, G.A. Jullien, and W. C. Miller, "A New Algorithm for the Elimination of Common Subexpressions in Hardware Implementation of Digital Filters by Using Genetic Programming," *Journal of VLSI Signal Processing*, vol. 31, no. 2, 2002, pp. 91-100.
13. W. Badawy and M. Bayoumi, "A Low Power VLSI Architecture for Mesh-based Video Motion Tracking," IEEE *Transactions on Circuits and Systems* II, vol 49, July 2002, pp. 488-504.
14. W. Badawy and M. Bayoumi, A Multiplication-Free Algorithm and A Parallel Architecture for Affine Transformation," *The Journal of VLSI Signal Processing-Systems*, Kluwer Academic Publishers, Vol 31, No 2, May 2002, pp. 173-184.
15. W. Badawy and M. Bayoumi, "Algorithm-Based Low Power VLSI Architecture For 2d-Mesh Video Object Motion Tracking", IEEE *Transaction on Circuits and Systems for Video Technology*, Vol 12, No. 4, April 2002, pp. 227-237

Accepted publications by refereed journals

1. L. Imbert, V.S. Dimitrov, and G.A. Jullien, "Fault-tolerant Computations over Finite Rings with Applications in Digital Signal Processing," IEEE *Trans. on Circuits and Systems* (paper TCAS1-0171, 2003, in press - 11 journal pages).
2. V.S. Dimitrov and G.A. Jullien, "Loading the Bases: A New Number Representation with Applications," invited article for IEEE *Circuits and Systems Magazine*, No. 2, July 2003 (in press).Alfred C. H. Yu and Wael Badawy, "A Novel Video Object Extraction Algorithm for Real-time Mesh based Motion Tracking Applications," IEEE *Transaction on Circuits and Systems for Video Technology* (in press).
3. W. Badawy and M. Bayoumi, "A Low Power VLSI Architecture for Mesh-based Video Motion Tracking," *The Journal of VLSI Signal Processing-Systems*, Kluwer Academic Publishers (in press - invited).

Refereed Conferences

1. A. Vetteth, K. Walus, G.A. Jullien, and V.S Dimitrov, "RAM Design Using Quantum-Dot Cellular Automata," Proc. 2003 NanoTechnology Conference, San Francisco, February 23-27, 2003, pp. 160-163.
2. P. Zhang and G.A. Jullien, "MEMS-based Micro-needle Structures for Biomedical Applications," Proc. 2003 NanoTechnology Conference, San Francisco, February 23-27.
3. K.A.Wahid, V.S Dimitrov, G.A. Jullien and W. Badawy, "An Analysis of Daubechies Discrete Wavelet Transform Based on an Algebraic Integer Encoding Scheme," IEEE Workshop on Digital and Computational Video, Clearwater, November 2002, (in press).
4. K.A. Wahid, V.S Dimitrov, G.A. Jullien, and W. Badawy, "An Algebraic Integer Based Encoding Scheme for Implementing Daubechies Discrete Wavelet Transforms," Proc. Asilomar Conference on Signals, Systems and Computers, (2002, in press - 5 pages).
5. A. Vetteth, K. Walus, V.S. Dimitrov, and G.A. Jullien, "Quantum-Dot Cellular Automata Carry-Look-Ahead Adder and Barrel Shifter," IEEE Emerging Telecommunication Technologies Conference, Dallas, September 23-24 2002, CD-ROM paper 2-I-4 (5 pages).

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7. I.C. Baykal and G.A. Jullien,"Detection of Defects in Textures with Alignment Error for Real-Time Line-Scan Web Inspection Systems," Proc. IEEE Mid-West Symposium on Circuits and Systems, August 2002, vol. 3, pp. 292-295.
8. V.S. Dimitrov and J.M.A Tanskanen,"Probabilistic design of long error-free fixed-point polynomial predictors and differentiators," IASTED International Conference on Signal and Image Processing, Kauai, August 2002, pp. 394-398.
9. G.A. Jullien, H. Li, R. Muscedere, and V.S. Dimitrov, "The application of 2-D logarithms to low-power hearing-aid processors," IEEE Mid-West Symposium on Circuits and Systems, vol. 3, 2002, pp. 13-16.
10. V.S Dimitrov, G.A. Jullien, and K. Walus, "Digital filtering using the multidimensional logarithmic number system," Proc. 47th Annual SPIE conference, Seattle, July 2002, (invited).
11. R. Muscedere, V.S Dimitrov, G.A. Jullien, and W.C. Miller, "Efficient Conversion From Binary to Multi-Digit Multi-Dimensional Logarithmic Number Systems using Arrays of Range Addressable Look-Up Tables," International Workshop on Application Specific Array Processors, San Jose, July 17-19, 2002, pp. 130-138.
12. M. Alam, W. Badawy, and G.A. Jullien, "A novel pipelined threads architecture for AES encryption algorithm," IEEE International Conference on Application-Specific Systems, Architectures and Processors, 2002, pp. 296 -302.
13. S. Chowdhury, M. Ahmadi, G.A. Jullien, and W.C. Miller, "MEMS Socket Interface For Soc Connectivity," 2nd IEEE Workshop on System-on-Chip for Real-Time Applications, Banff, July 2002, pp. 309-318.
14. A. Garg, G.A. Jullien, G.H. McGibney,* and J.W. Haslett, "Modulus Replication Complex Adaptive Filter IP Core," 2nd IEEE Workshop on System-on-Chip for Real-Time Applications, Banff, July 2002, pp. 430-437.
15. M. Alam, D. Onen, W. Badawy, and G.A. Jullien, "VLSI Prototyping of low-complexity wavelet transform on FPGA," IEEE Canadian Conference on Electrical and Computer Engineering, vol. 1, 2002, pp. 412-415.
16. M. Alam and W. Badawy, "VLSI Architecture Prototyping of Pipelined IIR Digital Filter" IEEE Canadian Conference on Electrical and Computer Engineering, vol. 2, 2002, pp. 1031-1035.
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18. R. Muscedere, I.C. Baykal, and G.A. Jullien, "On the use of Hash Functions for Defect Detection in Textures for In-Camera Web Inspection Systems," Proc. IEEE Int. Symp. on Circuits and Systems, vol. 5, 2002, pp. 665-668.
19. S. Chowdhury, M. Ahmadi, G.A. Jullien, and W.C. Miller, "A MEMS Socket System for High Density SOC Interconnection," Proc. IEEE Int. Symposium on Circuits and Systems, vol. 1, 2002, pp. 657-660.

Accepted papers at Refereed Conferences

1. A. Garg, I. Steiner, G.A. Jullien, J.W. Haslett, and G.H. McGibney, "A High Speed Complex Adaptive Filter for an Asymmetrical Wireless LAN Using a New Quantized Polynomial Representation," to be presented at the IEEE Int. Symp. on Circuits and Systems, Bangkok, May 2003.
2. Y. Wei, W. Badawy, "A NEW Moving Object Contour Detection Approach", to be presented at the 2003 IEEE international workshop on Computer Architectures for Machine Perceptions, May 12-14, 2003, New Orleans, USA.
3. Y. Wei and W. Badawy, "A Novel Zoom Invariant Video Object Tracking Algorithm (ZIVOTA)," to be presented at the 2003 IEEE Canadian Conference on Electrical and Computer Engineering, Montréal, Canada, May 4-7, 2003.

4. X. Liu and W. Badawy, "A Novel Error Control Scheme For Video Streaming Over IEEE802.11 Network," to be presented at the 2003 IEEE Canadian Conference on Electrical and Computer Engineering, Montréal, Canada, May 4-7, 2003.
5. P. Aggarwal, K. V. I. S. Kaler and W. Badawy, "Design and Implementation Of MEMS Based Micro-Needles For Biomedical Applications," to be presented at the 2003 IEEE Canadian Conference on Electrical and Computer Engineering, Montréal, Canada, May 4-7, 2003.
6. Alfred Yu and Wael Badawy, "On Reducing The Size Of Structured Meshes With A Novel Video Object Extraction Algorithm," to be presented at the 2003 IEEE Canadian Conference on Electrical and Computer Engineering, Montréal, Canada, May 4-7, 2003.
7. W. Khan, V.S Dimitrov, and G.A. Jullien, "Error-Free Arithmetic for Discrete Wavelet Transforms using Algebraic Integers," to be presented at the 16th IEEE Symposium on Computer Arithmetic (ARITH16), Spain, June 15-18, 2003.
8. M. Alam, C. A. Rahman, W. Badawy, and G.A. Jullien, " Efficient Distributed Arithmetic Based DWT Architecture for Multimedia Applications," to be presented at the 3rd IEEE Int. Workshop on System-on-Chip for Real-Time Applications, Calgary, June 30 - July 2, 2003.
9. Mohammed Sayed and Wael Badawy, "A New Class of Computational RAM Architectures for Real-Time MPEG-4 Applications," to be presented at the 3rd IEEE Int.l Workshop on System-on-Chip for Real-Time Applications, Calgary, June 30 - July 2, 2003.
10. J.R. Keilman, G.A. Jullien, and K.I.V.S. Kaler, "A SoC Bio-analysis Platform for Real-time Biological Cell Analysis-on-a-Chip," to be presented at the 3rd IEEE Int.l Workshop on System-on-Chip for Real-Time Applications, Calgary, June 30 - July 2, 2003.
11. M. Alam, W. Badawy, and G.A. Jullien, "Time Distributed DCT Architecture for Multimedia Applications," to be presented at the IEEE International Conference on Consumer Electronics (ICCE), Los Angeles, California, June 17-19, 2003.
12. P. Mokrian, G.A. Jullien, and M. Ahmadi, "Interconnect effects in deep submicron implementation of high performance arithmetic architectures," Advanced Signal Processing Algorithms, Architectures, and Implementations XIII, SPIE Annual Conference, August 2003.
13. K. Walus, G.A. Jullien, V.S Dimitrov, and A. Budiman, "Computer Arithmetic Structures for Quantum Cellular Automata," invited paper to be presented at the 2003 Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, Nov. 9-12, 2003.

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1. W. Badawy, and G.A. Jullien, (eds.), *System-on-Chip for Real-Time Applications: Concepts, Architectures and Implementations*, Kluwer Academic Publishers, 2002, ISBN: 1-4020-7254-6.

Other

Special Issues

1. G.A. Jullien, G.A. and M. Schulte (Guest Editors), "Special Issue on Application-specific Systems, Architectures, and Processors," *Journal of VLSI Signal Processing*, vol. 32, no. 2, 2002, pp. 75-184.

National Workshops

1. K. Walus, V. Dimitrov, G.A. Jullien, and W.C. Miller, "QCADesigner: A CAD Tool for an Emerging Nano-Technology," to be presented at the 2003 Micronet Annual Workshop, Toronto.
2. M. Amtoun, A. Razavi, M. Ahmadi, G.A. Jullien, and W.C. Miller, "Analysis and Simulation of a Single-lens Plenoptic Camera for Depth Extraction," to be presented at the 2003 Micronet Annual Workshop, Toronto.
3. J. Doherty, G.A. Jullien, and M.P. Mintchev, "Transcutaneous Powering of an Implantable Stimulator for Re-creation of Impaired Gastrointestinal Motility," Biomedical Engineering Workshop, Banff, November 2002.

4. J. Keilman, G.A. Jullien, and K.V.I.S. Kaler, "Design of an Arbitrary Electric Field Generator for use with a Dielectrophoretic Based Laboratory-on-a-Chip," Biomedical Engineering Workshop, Banff, November 2002.
5. K. Walus, R.A. Budiman, and G.A. Jullien, "Effects of morphological variations of self-assembled nanostructures on quantum-dot cellular automata (QCA) circuits," Frontiers of Integration, An International Workshop on Integrating Nanotechnologies, Edmonton, October 28, 2002.
6. K. Walus, A. Vetteth, G.A. Jullien, and V.S. Dimitrov, "Design and Simulation of Quantum Dot Cellular Automata," CMC Symposium On Microelectronics Research & Development In Canada, (This demonstration won the Micralyne award.) June, 2002.
7. S. Chowdhury, M. Ahmadi, G.A. Jullien, and W.C. Miller, "MEMS Based Connectivity for System Integration and Testing," Micronet Workshop, April, 2002.
8. R. Muscedere, J. Li, V.S Dimitrov, G.A. Jullien, M. Ahmadi, and W.C. Miller, "Multi-Dimensional Logarithmic Number Systems and Applications to Hearing Instrument Processors," Micronet Workshop, April, 2002.
9. M. Fu, V.S. Dimitrov, G.A. Jullien, M. Ahmadi, and W.C. Miller, "Implementation of an Error-Free DCT using Algebraic Integers," Micronet Workshop, April, 2002.

Contribution to Standards (2002-2003)

1. M. Alam, W. Badawy and G.A. Jullien. "Implementation & Hardware Reference Code for AMBA Bus Interface - Decoder (MPEG-4) IP Cores," ISO/IEC JTC1/SC29/WG11 MPEG2002/M8564
2. M. Alam, W. Badawy and G.A. Jullien. "MPEG-4 Video Hardware Reference Code for DCT & its Specifications for MPEG-4 Decoder," ISO/IEC JTC1/SC29/WG11 MPEG2002/M8565
3. M. Alam, W. Badawy and G.A. Jullien. "Integer DWT Reference Code and Specifications for MPEG-4," ISO/IEC JTC1/SC29/WG11 MPEG2002/M8582
4. ISO/IEC JTC1/SC29/WG11 N4965, Wael Badawy, Marco Mattavelli, and Robert Turney, Current development status of the MPEG4: Part 9 Reference Hardware Description.
5. ISO/IEC JTC1/SC29/WG11 MPEG2002/ M8562, Wael Badawy and Mohammed Sayed, "Embedded Memory Architecture For Motion Compensation in MPEG-4 Simple Profile"
6. ISO/IEC JTC1/SC29/WG11 MPEG2002/ M8563, Wael Badawy and Mohammed Sayed, "Motion Estimation Architecture for MPEG-4 Simple Profile"

Tutorials

1. W. Badawy, Y. Savaria, and G.A. Jullien, "System-On-Chip (SoC) Technology: The Future of VLSI Design," to be presented at the IEEE International Symposium on Circuits and Systems, Bangkok, May 2003.

COLLABORATION WITH ATIPS

RFIC DESIGN GROUP

We are entering a new age of ubiquitous wireless connectivity. Cellphone usage is targeted to hit hundreds of millions of users by 2002. New wireless networks like Bluetooth and WiFi - 802.11 seek to connect not only our cellphones, but also our laptops, PDAs, and even our home appliances. Inside each of these devices will be a wireless transceiver in integrated circuit form, a Radio Frequency Integrated Circuit (RFIC).

There are many challenges involved in creating RFICs. At the transistor level, various competing technologies (GaAs, Si, SiGe, and CMOS) each provide different benefits and drawbacks. Aside from the transistors, the creation of passive devices such as inductors, capacitors, and resistors also poses unique challenges to the IC designer. To create the amplifiers, mixers, and oscillators required in all wireless transceivers, RFIC designers must use clever circuit techniques to boost performance. These wireless "building blocks" can then be connected in different system architectures to achieve the required performance. The goal is to have a single radio-on-a-chip that need only to be connected to an antenna, output device, and a battery.

The ATIPS - RFIC research group is investigating solutions to many of the challenges presented above. Our research group is lead by IEEE Fellow Dr J.W. Haslett. The team currently consists of four PhD students, eight Master's students, and two Post Doctoral Fellows. We also work with Dr J. McRory who is both an Adjunct Professor with the University of Calgary and the Chief RF Scientist at TRLabs. Some of our past and present work includes:

- Developing solutions in state-of-the-art GaAs, CMOS, and SiGe technologies
- Creating innovative new structures for integrated capacitors and inductors
- A Tuneable, Active Inductor in both GaAs and CMOS implementations
- Analog signal processing circuits for smart antenna systems
- Circuit techniques for improved passive device performance
- A 4GHz logarithmic amplifier for fiber-optic applications
- High performance variable gain amplifiers for DSL wireline communications
- SiGe RFIC circuits for 4th generation wireless networks
- Novel Voltage Controlled Oscillators with improved phase noise

The ATIPS - RFIC research group has access to design and test equipment within the department, and at TRLabs in the research park adjacent to campus.